Richard Lee Bradley Jr.

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Summary

Hardware simulation/verification engineer with twelve years of experience working on large systems looking for contract position. My experience varies from designing system-level (multi ASIC) testbenches from the ground up to module-level. I have experience in various C++ based approaches, as well as Specman's e. I am a fast learner, and can quickly learn new languages or processes. I have unique experience, and a proven track-record.

Employment Experience

Exegy, Verification Manager, NOV 2006 – Current.

- Reinvented Exegy's verification environment to be more modular, portable, flexible, and easier to use, while maintaining old environments utility and feel.
  - Added functionality to the TEAL C++ open-source library to support desirable features.
    - Software-driven clocks, exit to command line, and properly working restart.
    - Made changes to get Teal to fully support compilation on AMD 64 bit chips.
  - Ported all existing tools to a more Object-Oriented format. Cleaned up many elusive bugs with older system.
  - Rewrote existing makefiles to be more test-centric.
- Created transaction level, directed random, Automatically checked test-benchs.
  - Created scripts to interface with preexisting data-dictionary to automatically generate transactions from software team's definitions.
  - Wrote multiple BFM's, directed-random stimulus generators, and transaction analyzers to support multiple products.
- Wrote testplan and executed testing for several products.
  - Created and maintained bulk of testcases.
  - Tracked errors.
  - Collected and helped analyze coverage information.
  - Ran regression tests.

Matisse Networks, Independent Contractor, Dec 2004 – May 2006.

- Responsible for verification of several modules/sub-system of optical switch.
- Wrote testplans, and held group reviews of those plans.
- Scheduled work to be done.
- Designed/coded testbench (C++, TestBuilder).
- Ran/debugged tests.
- Modules tested: queue management module, MAC table lookup module, packet reassembler, and ingress subsystem.

- Tracked bugs found in testing. Worked with designers and management to ensure no issues were missed.
- Supported product in the lab by reproducing issues in simulation.

Senetric, Independent Contractor, Dec 2003 – March 2004.

- Created low-level Java interface and API for RFID system.
- Created GUI controller for RFID demo system.

Erlang Technology, Design Engineer. July 2001 – July 2003

- Lead designer in verification of "Core" switch-fabric device.
- Responsible for design, testing, coding, and maintenance of product simulation software using object-oriented analysis and design techniques with Verisity's 'e' language.
- Executed pre-silicon testing of product.
- Two ASIC designs, no major functional bugs in final product.

Celox Networks, Lead Design Verification Engineer. November 1999 – July 2001

- Designed simulation software to exercise Celox SCx 4800 service-creation switch at the system (multi-chip) level using a mixture of C++, C, Verilog and embedded Perl under severe time considerations. (Product was a loosely coupled 16 - 512 processor system with specialized "network processor" ASICs.)
- Coordinated team of 8-12 people creating test-bench.
- Built Verification team from 2 to 7 engineers.
- Worked at key contractor sight in India to coordinate 5-10 person testing team with development team based in USA.
- Involved with the design, coding, and maintenance of test bench, debugging and tracking of HW tests, plotting strategy and evaluating potential new techniques and processes for design and verification.
- Three ASICS designs, no respins.

Hewlett Packard, Design Verification Engineer. August 1997 -- November 1999

- Designed software model of a processor to be used as simulation test stimulus. (HP's PA-RISC processor.) using C++.
- Performed system-level testing of 1 to 128 processor ccNUMA computer systems (HP 9000 V2500.) Created both random and directed simulation tests.
- Developed system-level test requirements for PCI based IO and error testing from hardware documentation.
- Involved with verification of proprietary table-based coherency scheme, SCI coherency, Fault cases, PCI based I/O, Packet routing, memory configurations, physical configurations, dead locks, and hardware-supported semaphore.
- Supported lab bring up by finding and identifying lad bugs in simulation.
- Developed/maintained tools to support the system simulation effort.
- Developed random system simulation IO exerciser in Perl.
- Five ASIC designs, one respin of one chip.

Texas Instruments/Raytheon, Test Engineer. August 1996 -- August 1997

- Developed UNIX based software that delivered digital video to UUT.

- Created low-level software to communicate with proprietary R/F device.
- Designed pulse-width-modulated circuit to interface prototype product.
- Wrote code to perform functional tests on proprietary multi-processor computer system.

Education

University of Missouri--Columbia, Major: Computer Engineering
Bachelor of Science, August 1996

Skills/Experience

C/C++	Java	Design Patterns	Verification
Testbuilder	UML	Perl	Verilog
SystemC	Object-Oriented A/D	Test Plans	
Specman's E		UNIX/Linux	